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L36 L35 and ((reallocate\$3 or re-alloc\$3) adj5 portion adj5 cache) 1 L36

L35 ((711/104 |711/105 |711/115 |711/165 |711/170 |711/172 |711/173
 |711/129 |711/153 |711/154 |711/171)!.CCLS.) 3596 L35

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L34 L32 and (cach\$3 adj3 director\$3) 3 L34

L33 L32 and (cache adj3 director\$3) 2 L33

L32 (5276832.pn.) or l29 or l28 or l24 or l23 90 L32

L31 5276832.pn. and remov\$ 1 L31

L30 L29 and remov\$ 2 L30

L29 5784548.pn. 2 L29

L28 (removabl\$5 adj3 cache) 30 L28

L27 (removabl\$5 adj3 dram) 4 L27

L26 l4 and (removabl\$5 adj3 dram) 1 L26

<u>L25</u>	L24 and (((plug adj3 play) or (hot adj2 swap\$5)) with memor\$3))	0	<u>L25</u>
<u>L24</u>	6098132.pn. or 5943482.pn. or 6101322.pn.	6	<u>L24</u>
<u>L23</u>	118 and (((plug adj3 play) or (hot adj2 swap\$5)) with memor\$3))	52	<u>L23</u>
<u>L22</u>	120 or L21	9	<u>L22</u>
<u>L21</u>	(((hot adj2 remov\$3)) with memor\$3)).ab,ti.	5	<u>L21</u>
<u>L20</u>	(((hot adj2 add\$3)) with memor\$3)).ab,ti.	4	<u>L20</u>
<u>L19</u>	20020069322.pn.	2	<u>L19</u>
<u>L18</u>	(((plug adj3 play) or (hot adj2 swap\$5)) with memor\$3)).ab,ti.	52	<u>L18</u>
<u>L17</u>	(((plug adj3 play) or (hot adj2 swap\$5)) same memor\$3)).ab,ti.	89	<u>L17</u>
<u>L16</u>	(((plug adj3 play) or (hot adj2 swap\$5)) and memor\$3)).ab,ti.	144	<u>L16</u>
<u>L15</u>	L10 and (cach\$3 adj3 director\$3)	1	<u>L15</u>
<u>L14</u>	L12 and (cach\$3 adj3 director\$3)	4	<u>L14</u>
<u>L13</u>	L12 and (cach\$3 adj3 director\$3)	4133	<u>L13</u>
<u>L12</u>	(((plug adj3 play) or (hot adj2 swap\$5)) same cach\$3)	55	<u>L12</u>
<u>L11</u>	(((plug adj3 play) or (hot adj2 swap\$5)) adj3 memor\$3)	56	<u>L11</u>
<u>L10</u>	(((plug adj3 play) or (hot adj2 swap\$5)) with memor\$3)	357	<u>L10</u>

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<u>L9</u>	L6 and (((plug adj3 play) or (hot adj2 swap\$5)) with memor\$3)	0	<u>L9</u>
<u>L8</u>	L6 and ((plug adj3 play) adj5 memor\$3)	0	<u>L8</u>
<u>L7</u>	L6 and ((hot adj2 swap\$5) adj5 memor\$3)	0	<u>L7</u>
<u>L6</u>	L4 and ss-dasd	0	<u>L6</u>
<u>L5</u>	L4 and ssdasd	0	<u>L5</u>
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<u>L3</u>	((711/104 711/105 711/115 711/165 711/170 711/172 711/173)!.CCLS.)	2469	<u>L3</u>
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System Sciences, 1997, Proceedings of the Thirtieth Hawaii International Conference on , Volume: 5 , 7-10 Jan. 1997

Page(s): 168 -177 vol.5

[\[Abstract\]](#) [\[PDF Full-Text \(972 KB\)\]](#) **IEEE CNF****2 Multicast with cache (Mcache): an adaptive zero-delay video-on-demand service***Ramesh, S.; Injong Rhee; Guo, K.;*

INFOCOM 2001. Twentieth Annual Joint Conference of the IEEE Computer and Communications Societies. Proceedings. IEEE , Volume: 1 , 22-26 April 2001

Page(s): 85 -94 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(608 KB\)\]](#) **IEEE CNF****3 Role of download time as a key in Web cache management policies***Fonseca, N.L.S.; Oliveira, R.M.;*

Global Telecommunications Conference, 2001. GLOBECOM '01. IEEE , Volume: 3 , 25-29 Nov. 2001

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5 Reducing cache conflicts by partitioning and privatizing shared arrays

Zhiyuan Li;

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6 Coordinating simultaneous caching of file bundles from tertiary storage

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Digital Avionics Systems Conference, 1997. 16th DASC., AIAA/IEEE , Volume: 1 , 26-30 Oct. 1997

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[\[Abstract\]](#) [\[PDF Full-Text \(548 KB\)\]](#) **IEEE CNF****3 The Windows NT kernel architecture***Solomon, D.A.;*

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1 The effect of residual adsorbed gases on silicon isotope amount ratio measurements [in Avogadro constant determination]*Valkiers, S.; Gonfiantini, R.; Taylor, P.; De Bievre, P.;*

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4 Development of a new wearable multi-channel sensing unit

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5 An instrument with a DSP for monitoring human biological parameters

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9 A smart bolter for improving entry stability*Howie, W.L.; Frizzell, E.M.;*

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10 VLSI echo cancellation filter*Akiwumi-Assani, O.; Potu, B.;*

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11 Modelling of a trellis decoder used as inner code in a concatenated coding system*Ferland, G.;*

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13 Removal of memory access bottlenecks for scheduling control-flow intensive behavioral descriptions*Ravi, S.; Lakshminarayana, G.; Jha, N.K.;*

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14 BIST diagnostics. I. Simulation models*Savir, J.;*

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19 A transistorless-current-mode static RAM architecture
Levy, H.J.; Daniel, E.S.; McGill, T.C.;
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20 Equilibrium characterization of dynamical neural networks for synthesis of associative memories

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24 An efficient incremental algorithm for identifying consistent checkpoints

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25 A challenge over 100 Gbit/in² rewritable/removable MO storage

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26 Semi-asynchronous checkpointing for optimistic simulation on a Myrinet based NOW

Quaglia, F.; Santoro, A.;

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Wang Jun; Mao Shiyi; Wang Yuezhong;

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28 Software quality classification modeling using the SPRINT decision tree algorithm

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29 A board system for high-speed image analysis and neural networks

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Jae-Wook Lee; Myung-Hoon Yang; Sungho Kang; Yoonsik Choe;

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